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with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1A through 1D are diagrams to explain
5 conventional steps of fabricating a capacitor element
having a via terminal;

FIG. 2 is a cross-sectional view of a
semiconductor device substrate according to an embodiment
of the present invention;

10 FIG. 3A is an enlarged view of a portion of the
semiconductor device substrate shown in FIG. 2;

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FIGS. ~~3A~~⁸ and ~~3B~~⁶ are cross-sectional views of the
semiconductor device substrate with respect to a BB plane
and a CC plane, respectively, illustrated in FIG. ~~3A~~³;

15 FIG. 4 is an enlarged view of an exemplary
structure of a via terminal shown in FIG. 3A;

FIG. 5 shows an exemplary structure of a
semiconductor device having the semiconductor device
substrate shown in FIG. 2;

20 FIGS. 6A through 6D are diagrams to explain
fabrication steps of fabricating a semiconductor device
substrate according to an embodiment of the present
invention;

FIGS. 7A through 7C are diagrams to explain
25 subsequent fabrication steps according to an embodiment of
the present invention;

FIGS. 8A through 8C are diagrams to explain
subsequent fabrication steps according to an embodiment of
the present invention;

30 FIGS. 9A through 9D are diagrams to explain
subsequent fabrication steps according to an embodiment of
the present invention;

FIGS. 10A through 10D are diagrams to explain